ABSTRACT

A serially programmable integrated circuit (IC) includes a memory array and multiple data registers daisy-chained by bypass logic. Each of the data registers is associated with a primary column grouping or redundant column grouping in the memory array. If a data register is associated with a primary column grouping that includes a defective column, the bypass logic bypasses that data register and incorporates one of the data registers associated with a redundant column grouping into the serial programming path of the IC. Therefore, when a programming bitstream is shifted into this serial programming path, defective columns in the memory array are automatically bypassed during the subsequent programming operation. To read a word from the memory array, any data stored in the redundant columns is first read out, and then the data from the primary columns is read out, bypassing the previously identified defective column groupings.